EXHIBIT 4

EXHIBIT B

AND8248/D

System Clock Generators: A Comparison of a PLL Synthesizer vs. a Crystal Oscillator Clock

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APPLICATION NOTE

Abstract
An electronic system requires a reliable, precision timing reference: the system clock. We examine and compare two forms of system clocks, the Crystal Oscillator and the Phase Locked Loop Synthesizer.

The System Clock

Generation and distribution of the system master clock will require at minimum an oscillator source driving a gain amplifier, translation to standard logic levels, and a clock distribution network. Two of the most common oscillator sources are the Crystal Oscillator Clock Module and the Phase Locked Loop (PLL) Synthesizer Clock. A complex system clock may include: a mux function between oscillator sources, additional translation to other logic family levels, fanout buffering, zero delay buffering, skew tuning, higher multiple frequency generation, and frequency division in diverse topologies. See Figure 1: Generic System Clock Tree Design illustrating various possible topologies and applications of On Semiconductor devices in a system clock tree.

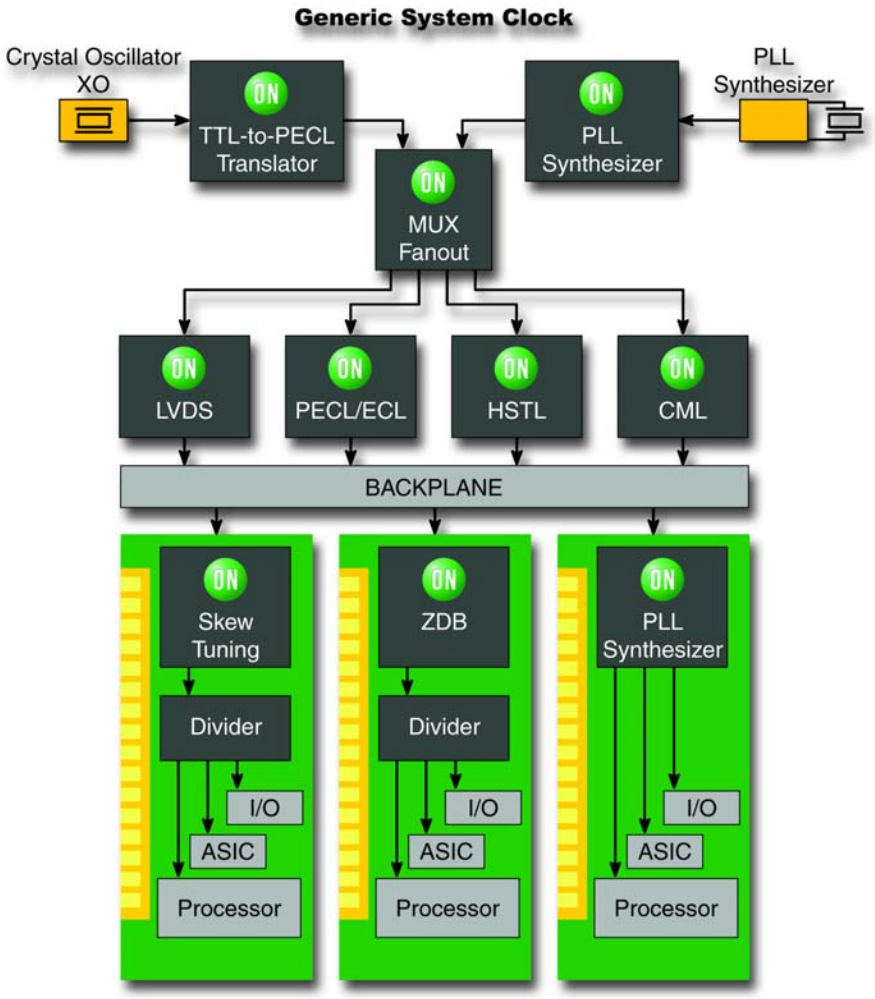

Figure 1. Generic System Clock Tree Design

Today's very complex system designs may need to distribute numerous clock copy signals at several logic standards and at several frequencies. Some boards may also demand tight skew and synchronization characteristics between several devices requiring zero delay buffers and skew tuning buffers. Multiple copies of a clock may require a fanout buffer for distribution. Frequency multiples of a clock may require a PLL synthesizer. All these requirements may be combined in challenging clock tree designs.

Crystal Oscillator Clock (XO)

The traditional System Clock Tree oscillator source in general use is a quartz crystal. For oscillator operation, the quartz crystal must also be in a loop with a gain amplifier to compensate for crystal losses and to match impedances. This gain amplifier must also be level translated to standard logic levels for use by the system clock distribution network. For a generalized schematic of the Crystal Oscillator Clock, see Figure 2: Typical Crystal Oscillator Clock.

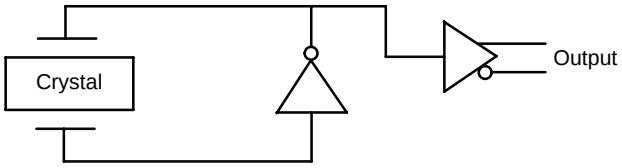

Figure 2. Typical Crystal Oscillator Clock

A Crystal Oscillator Clock (or XO) is usually found as a single supply hermetically sealed, or "canned", module with an internal crystal and integrated circuitry, although a discrete hybrid remains an alternative design. These canned oscillators are complex to manufacture and may be relatively expensive with long lead times and unique custom customer requirements often driving cost higher. The Crystal Oscillator Clock is generally limited to a single frequency and only one logic output, or a single differential pair. Operation may be in a fundamental or overtone mode.

Key characteristic features of the Crystal Oscillator Clock may include:

- Frequency Accuracy
- Frequency Precision
- Stability across temperature and voltage
- Oscillation startup time
- Aging
- Jitter (Phase Noise, Cycle−to−Cycle, Period)
- Output load capability
- Duty Cycle
- Rise and fall times
- Power Dissipation or current demand

Some advantages may include:

- Crystal ease of use
- Frequency Accuracy and Precision
- Family logic level compatible output

Some disadvantageous limitations may include:

- Crystal fixed operating frequency
- Single Output
- Custom order application specific frequencies
- Large physical size
- Long delivery lead time

PLL−Synthesizers

A more advanced System Clock Tree oscillator source is a Phase Locked Look Synthesizer clock generator offering greater design flexibility and potential cost reduction. By utilizing fully integrated Phase Locked Loop (PLL) circuitry, higher functions become available such as multiples of the crystal frequency, and output phase alignment. A single Synthesizer clock device could offer substantial cost reduction over a design with multiple crystals of different frequencies. ON Semiconductor PLL−synthesizer clock generators offer comparable or better parametric performance, greater design flexibility, a lower overall cost potential, and reduced lead times compared to the most widely used crystal oscillators. For a generalized schematic of a simple PLL Synthesizer Clock Generator, see Figure 3: Typical PLL Synthesizer Clock.

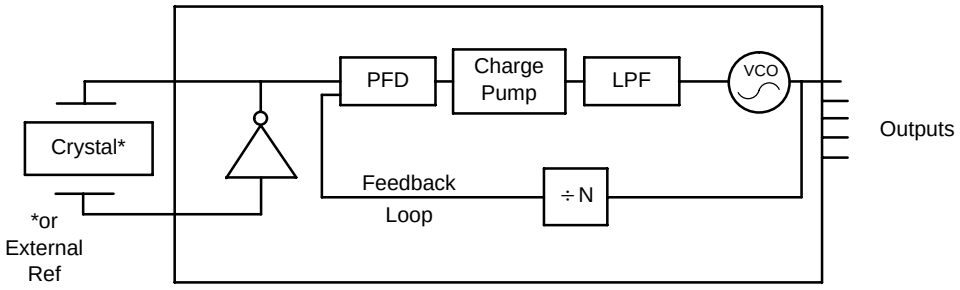

Figure 3. Typical PLL Synthesizer Clock

A generic PLL Synthesizer Clock device requires an external crystal and contains an integrated phase−lock−loop (PLL) circuit capable of multiplying up or dividing down the crystal's unique frequency. An external crystal permits the added flexibility of fine−tuning or pulling frequency, but requires additional external stabilizing capacitors, one on each side of the crystal.

For operation, the quartz crystal must also be in a loop with a gain amplifier to compensate for crystal losses and to match impedances. This gain amplifier output becomes a Reference signal to the Phase Frequency Detector (PFD) which drives a charge pump and a Low Pass Filter (LPF). The LPF output approaches a DC level which drives the Voltage Controlled Oscillator (VCO) at frequency. Output from the VCO may be ported out of the device, but will also be sent through a Divide counter (÷N) and back to the PFD as a Feedback signal. As a loop dynamic, the PFD compares the Feedback signal to the Reference and outputs a pulse width modulated signal to pump the VCO frequency/phase either up or down, accordingly to the crystal Reference. The Charge Pump assures the pulse width modulated signal will not vary in the HIGH and LOW levels. The "÷N" counter will multiply up the VCO output frequency. For "Phase Lock Loop General Operations", see AND8040.

Common to all PLL outputs, the VCO output phase approaches zero with respect to the input Reference signal (zero delay buffering). When the PLL feedback loop "÷N" is externally accessibly, controlled delay may be added. More complex PLL Synthesizer devices may incorporate multiple PLLs, additional input or output dividers, logic family translators, or banks of fanout. The VCO output must also be level translated to standard logic levels for use by the system clock distribution network.

Key characteristic features of a generic PLL Synthesizer Clock include all those of the Crystal Oscillator Clock:

- Frequency Accuracy
- Frequency Precision
- Stability across temperature and voltage
- Oscillation startup time
- Aging
- Jitter (Phase Noise, Cycle−to−Cycle, Period)
- Output load capability
- Duty Cycle
- Rise and fall times
- Power Dissipation or current demand

And additionally,

- Multiple Outputs
- Aligned Outputs
- Multiple Selectable Frequencies
- Pullable Frequency
- Jitter Rejection

Some advantages of the PLL Synthesizer Clock include all those found in the Crystal Oscillator Clock:

- Ease of use
- Frequency accuracy and precision
- Family logic level compatible output

And potential benefits:

- Lower frequency (less costly) crystal
- Multiple logic family outputs
- Differential outputs
- Multiple selectable frequencies
- Spread spectrum option
- Layout board area optimization (reduced overall footprint)
- Pullable Frequency
- Jitter Rejection
- Shorter delivery lead time
- Simplifies customer BOM

Some challenges may include:

- Crystal capacitor considerations

Frequency Accuracy and Stability

Frequency is exactly defined as the number of oscillations per second, but is often approximated as instantaneous frequency (reciprocal of the wavelength period) measurement with significant error. Frequency precision refers to the number of significant digits in a frequency measurement.

Output Frequency (Fout) accuracy is a marginal error (deviation boundary) from a nominal or mean spec value (Fin) and usually expressed in Parts Per Million (PPM). Crystal operation accuracy is typically measured at 25°C, where effects due to changes in operating temperature, input voltage, aging shock and vibration are most stable.

Frequency stability is typically expressed in Parts Per Million (PPM). It is as spec deviation boundary from a reference frequency over such parameters such as temperature, voltage, and time (drift and aging). Common crystal spec stability values overvoltage and temperature are 25, 50 and 100 PPM.

A crystal driven PLL frequency synthesizer would be phase and frequency locked on the crystal signal, thus retaining the crystal spec stability and accuracy in PPM. In a PLL the mean output frequency, fout, is a multiplier factor, N, of the input reference mean frequency:

$$Fout = (N)(Fin) \quad \text{(eq. 1)}$$

Where:

- Fout is the mean output frequency (in MHz)
- N is the multiplier factor
- Fin is the input reference mean frequency (in MHz)

A PLL output signal frequency accuracy, Fouta, expressed as ± PPM (parts per million) deviation relative to the output target mean frequency is equal to the input accuracy expressed as ± PPM deviation relative to the input target reference mean frequency. This due to the PLL locking both phase and frequency to the input signal.

$$\text{Fouta (output frequency } \pm \text{ PPM)} = \text{Fina (input frequency } \pm \text{ PPM)} \quad \text{(eq. 2)}$$

Where:

Fouta is the output deviation (± PPM relative to the output target mean frequency)

Fina is the input deviation (± PPM relative to the input target reference mean frequency)

If the input signal deviates ± 20 PPM from the input mean frequency, the output reference will deviate ± 20 PPM from the output mean frequency, regardless of the PLL's N loop multiplier factor. When frequency accuracy boundaries are expressed in Hertz (or MHz), they get multiplied by N, the PLL loop multiplier factor.

For example:

An NB4N507 PLL with a multiplier factor of 8 has an input reference crystal frequency of 16 MHz with ± 20 PPM accuracy. What is the output accuracy and frequency?

The output mean frequency, Fout, will be Fin times 8, the multiplier factor according to Equation 1.

$$\begin{aligned} \text{Fout} &= (\text{N})(\text{Fin}) \\ &= 8\,(16 \times 10 \,\wedge\, 6) \\ &= 128\ \text{MHz} \end{aligned}$$

Since the mean input frequency (Fin) of 16 MHz signal has the accuracy, Fa, of ± 20 PPM, the input signal deviation Fina is ± 320 Hertz:

$$\begin{aligned} \text{Fina} &= (\text{Fin})(\text{Fa}) \qquad \text{(eq. 3)} \\ &= (16 \times 10 \,\wedge\, 6)(\pm\ 20 \times 10 \,\wedge\, -6) \\ &= \pm\ 320\ \text{Hertz} \end{aligned}$$

The crystal frequency will range from 16.00032 MHz (or 16,000,320 Hz) to 15.99968 MHz (or 15,999,680 Hz).

Output frequency signal (Fout) of 128 MHz also has accuracy, Fa, of ± 20 PPM, and will deviate ± 2560 Hertz:

$$\begin{aligned} \text{Fouta} &= (\text{Fout})(\text{Fa}) \qquad \text{(eq. 4)} \\ &= (128 \times 10 \,\wedge\, 6)(\pm\ 20 \times 10 \,\wedge\, -6) \\ &= \pm\ 2560\ \text{Hertz} \end{aligned}$$

The output frequency will range from 128.00256 MHz (or 128,002,560 Hz) to 127.99744 MHz (or 127,997,440 Hz). Precision was not considered in this example.

Jitter

A stable PLL−based frequency synthesizer will display output frequency stability primarily determined by the crystal specifications, while presenting a characteristic additive Rj (random jitter) magnitude greater than the crystal spec. Output Jitter magnitude may be specified as Rj(RMS), Cycle−to−Cycle (RMS), Period (RMS), or total jitter (Peak−to−Peak) is measured time units, typically as ps.

Random Jitter (Rj) is a stochastic deviation in the edge placement from an ideal reference. This measurement is often made in the time domain on an accumulation of instantaneous waveforms (typ. 10,000). When measuring frequency, true Gaussian Rj (random jitter) is always present and must always sum to zero, whereas the magnitude measurement of Rj (random jitter) is an independent parameter to frequency. Period jitter is an accumulation (typ. 10,000) of instantaneous deviations in the waveform period from ideal reference locations

Alternatively, the jitter measurement may be derived from frequency domain Phase Noise summation, usually across a specified offset measurement frequency band from the ideal reference, or carrier. Sampling time close to the carrier becomes impractically long, limiting the measurement band lower cutoff. The upper measurement band cutoff becomes limited by approaching the residual noise floor.

Any crystal shock or vibration can produce large phase deviations. Supply noise, crosstalk, and EMI can affect jitter.

Summary

A System Clock Tree may consist of one or several Crystal Oscillator Clocks (XOs) which may be replaced by a PLL Synthesizer Clock and divider. Each PLL Synthesizer Clock output frequency may be further divided down to provide a replacement for two or more different Crystal Oscillator Clocks (XOs).

EXAMPLE 1)

DESIGN A has four separate Crystal Oscillator Clocks (XOs) and four Xtals:

(2) 16 MHz XO
(1) 32 MHz XO
(1) 128 MHz XO

Compared to DESIGN B with one Crystal Oscillator Clock (XOs) and one Xtal:

(1) 16 MHz Xtal on NB4N507 PLL with X8 selected for 128 MHz
(1) NB6L230 ÷ 4 (32 MHz) and ÷ 8 (16 MHz)
(1) MC100EP11 (1:2 Fanout of 16 MHz)

EXAMPLE 2)

DESIGN C has three separate Crystal Oscillator Clocks (XOs) and three Xtals:

(1) 200 MHz XO
(1) 100 MHz XO
(1) 50 MHz XO

Compared to DESIGN D with one Crystal Oscillator Clock (XOs) and one Xtal:

(1) 25 MHz Xtal on NB4N507 PLL with X8 selected for 200 MHz
(1) Use the 200 MHz into a MC100LVEP34 with ÷ 2 (100 MHz) and ÷ 4 (50 MHz)

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